REMARKS

Claims 1-11 and 14-17 are pending in the present application. Claims 1-10 and 14-17 are rejected under 35 U.S.C. § 102(b) as being anticipated by Johnson, U.S. Patent No. 5,898,701. Claim 11 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Johnson in view of Lindholm, U.S. Patent No. 6,553,523.

In response to the rejection of the claims, Applicant respectfully requests favorable reconsideration of the claims and withdrawal of the pending rejections. It is suggested in the Office Action that Claim 1 is disclosed in the Abstract and column 2, lines 19-22 of Johnson. However, there is no mention of a boundary scan register in the Abstract, and col. 2, lines 19-22 discloses a boundary scan register of a conventional JTAG circuit. In contrast to Applicant's claims, Johnson is directed to system of testing a circuit using a reduced number of method steps, instructions and clock cycles by using a combined address/data register, and expressly states that the boundary scan registers are shown as a part of a conventional device and are not necessary to practice the invention of Johnson. In particular, Johnson discloses the use of a combined address/data register which allows access to design-specific test support features in a device under test. By using a combined address/data register as shown in Fig. 4 of Johnson, the device under test may be tested using fewer steps. (Col. 5, lines 49-61). For example, as shown in Fig. 9 of Johnson, the device may be tested using only five method steps compared to seven method steps, and three instructions compared to four instructions required using the prior art device of Fig. 3. By reducing the number of methods and instructions, the implementation of Fig. 4 of Johnson reduces errors due to system noise and increases the testing throughput.

In contrast to data registers or the combined address/data registers, boundary scan registers allow testing of the board interconnections, testing of typical production defects such as opens and shorts, and access to component inputs and outputs. (Col. 5, lines 15-23). That is, boundary scan registers are associated with input/output (I/O) pins on an integrated circuit, and allow data on the I/O pins to be accessed through the JTAG interface. When a programmable logic device is being configured to perform a specific function, a configuration device transfers configuration data to the programmable logic device by way of a predefined interface. Accordingly, by using

boundary scan registers as claimed by Applicant, it is possible to capture configuration process signals during the configuration process during the configuration process, as claimed in each of the independent Claims 1, 9, 16 and 17. Such a use of boundary registers allows the analysis of data applied to an I/O pin of an programmable logic device, such as a connection providing configuration processing signals from a configuration device to a programmable logic device, for example. The use of data registers would not allow the analysis of configuration process signals applied to an I/O pin of the programmable logic device. There is simply no teaching or even a suggestion in Johnson that boundary scan registers are used to capture configuration process signals as claimed. Further, Johnson expressly states that the bypass register and boundary scan register function in a similar manner as in a conventional device, and are not required in order to practice the invention of Johnson. (Col. 5, lines 29-33).

In response to the rejection of Claim 11, Applicant respectfully submits that Claim 11 is allowable over the combination of references for the same reasons that Claim 9 is believed allowable over Johnson alone. That is, Lindholm is cited for disclosing that a field programmable gate array is a programmable logic device. However, Lindholm also fails to disclose or suggest a configuration analyzer analyzing configuration process signals stored in boundary scan registers of the programmable logic device during the configuration process, as claimed in independent claim 9. Applicant respectfully requests reconsideration of Claim 11.

Conclusion

Applicant believes that Claims 1-11 and 14-17 are in condition for allowance, and allowance of the application is therefore requested. If action other than allowance is contemplated by the Examiner, the Examiner is respectfully requested to telephone Applicant's attorney, Justin Liu, at 408-879-4641.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, Alexandria, VA 22313-1450, on April 10, 2007.

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